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13. ABSTRACT *(Maximum 200 words)*

We have investigated MISFETs based on GaAs, InGaAs, and InP materials with promising potential for microwave and high speed digital applications. Using state-of-the-art MBE and vacuum connected UHV CVD, the gate dielectric layer was deposited without exposing the surface to contaminants. The insertion of a thin layer of Si between theSi_3N_4 and GaAs and other II-V compounds led to improved interfaces. The gate dielectric quality in terms of low leakage and high breakdown volatge has been improved to a level comparable to that achieved by the thermal CVD method which must be performed at high temperatures not accessible by compound semiconductors. Our effort is directed toward the eventual realization of inversion-mode devices analogous to the traditional IC processing technologies.

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During last three year we have made significant progress in the field of Metal-Insulator-Semiconductor Field-Effect Transistors (MISFETs). Our objects in this investigation was to uncover the physics underlying electrical performance, technology and know-how of GaAs MISFETs. The knowledge gained from this study demonstrates that the realization of superior performance of GaAs based FETs in switching and power applications by employing an MIS structure is a real possiblility, and that the prospect of fabrication of singular and complementary MIS devices, and circuits for commercial use should no more be automatically ruled out.

Since this project started, we have studied a number of MIS structures, including Si_3N_4/Si/GaAs, Si_3N_4/Si/Ge/GaAs, Si_3N_4/Si/InGaAs/GaAs, Si_3N_4/Si/AlGaAs/GaAs, Si_3N_4/Si/GaP/GaAs, Si_3N_4/Si/SiO_2/GaAs structures. By employing novel MIS structures which utilize, silicon interface layer or a composite Si/Ge layer grown on GaAs, and a Si_3N_4 dielectric layer, we demonstrated that device structures with interface trap densities as low as mid 10^{10} $eV^{-1}cm^{-2}$ can be realized. It is not secret that key to the success of MOSFET technology is the high quality of silicon/insulator interfaces. Unlike the oxide growth process employed in Si technology, the insulators, such as Si_3N_4 and SiO_2, on III-V semicondutor need to be deposited at low temperatures using plasma-assisted technology. The unique deposition apparatus that has been installed in our laboratory, has proved that it is not only possible to maintain a highly contamination-free environment for the depostion of gate-quality insulators on III-V compound semiconductors, but also to obtain plasma-assisted insulator/semiconductor interfaces with remarkably low interface states. The insulator thickness of the MISFET structures grown in our laboratory is about 150 Å, and uniformity of the insulator surface is very high. All these have allowed our devices to be almost free of problems such as frequency dispersion, and hysteresis, and to yield marginally low gate leakage and high transconductance. Our study indicates that the gate leakage of GaAs MISFETs is lower than that of GaAs MESFETs by more than two orders of magnitude. It has been concluded that, in order to fabricate GaAs MISFETs, the first necessary step is to make a GaAs structure with unpinned GaAs surface Fermi level, and then to choose suitable surface preparation techniques. Thus it found that a sample preparation involving combined procedure for the MBE growth of III-V semiconductors (such as GaAs, InGaAs, InP, etc) and elemental semiconductors (e.g., Si, Ge, etc.), in situ sample transfer, and UHVCVD deposition of the insulator is vital to the success of III-V compound semiconductor MISFETs. A short and low temperature rapid thermal annealing of the sample should lead to the best possible results for them.

Our study of Si/SiGe modulation-doped structures was quite illimunating. We demonstrated that if an unusually thin and graded SiGe buffer layer is incorporated in the MBE grown Si(strained)/$Si_{0.7}Ge_{0.3}$ modulation-doped structure the density of threading dislocations is reduced by an order of magnitude, and the Hall mobility is increased to about 1800 cm^2/V.s at 300K and to 19,000cm^2/V.s at 77K. This may be considered as a major impediment to achieving high-electron mobility modulation-doped FETs (MODFETs). While studying Si/Ge MODFETs, we noted that negative differential resistance (NDR) occurs at gate biases above a certain threshold voltage, and that the drain voltage for the onset of NDR is dependent on the Schottky gate bias. Fundamental analyses suggest that a real space transfer of electrons from the strained Si channel to adjacent SiGe layers may be the primary cause of NDR in Si/SiGe MODFETs.

We performed experimental investigations of the effect of doping dependent bandgap grading on the uniformity of current gain in AlGaAs/GaAs heterojunction bipolar transistors. Our study indicates that an optimized doping gradient both in the emitter and the base results in improved uniformity of current gain with respect to collector current. This

study also indicates that the optimized doping gradient leads to a suppression of emitter size effects encountered in the scaling down of transistors.

In an attempt to understand the potentials of silicon carbide based bipolar transistors we carried out some a theiretical investigation to estimate their high-frequency and low-power performance. Both 6H-SiC homojunciton bipolar transistors (BJTs) and 6H-SiC/3C-SiC heterjunction bipolar transistors (HBTs) were studied for a temperature range of 27°C through 450°C. The results of our simulations demonstrate that ohmic contact resistance tends to limit the high-frequency performance of both SiC BJTs and HBTs.

In this final report, we are going to emphasize our effort in the in-depth investigations of the metal-insulator structures intended for semiconductor field-effect-transistors (MISFETs). An extensive study of the current conduction mechanism in the gate dielectrics consisting of stoichiometric Si_3N_4, Si rich Si_3N_4 or SiO_xN_y was undertaken and deposition conditions leading to dielectrics with the smallest leakage current, largest breakdown fields established. Moreover, the effect of in situ annealing on the Si interlayer, the quality of which is most crucial in determining the resulting dielectric and interfacial properties, and in turn its impact on the device characteristics as pertained to transconductance, electrical activity of SiN_x and SiO_xN_y films formed as gate dielectrics. Additional investigations are pertained to passivation of GaAs surface by anodic sulfide treatments and MISFET deive modeling and simulation.

For our Si_3N_4/Si/GaAs type MIS structure, the Si interlayer is crucial to the interface properties. However, Si epilayers grown at low temperatures (<450°C) lack the quality needed. An increase in growth temperature certainly improves the quality of Si, but also leads to a higher desorption rate of As from the GaAs surface. In order to circumvent the dilemma, we employed a new approach: low temperature deposition (300°C) and in situ anneal of the as-deposited Si (650°C). Low temperature Si deposition ensures the stoichiometry of GaAs, and the high temperature annealing improves the quality of Si. The samples with this in situ annealing step showed excellent and reproducible interfacial properties. The interface trap densities are around 9×10^{10} $eV^{-1}cm^{-2}$.

By employing Si interlayer or a composite Si/Ge layer in between GaAs and Si_3N_4 dielectrics, we have demonstrated the MIS structure capacitors with interface trap density as low as mid $10^{10}eV^{-1}cm^{-2}$. In the meanwhile, we have achieved the transconductance as high as 220mS/mm for a 5μm gate length GaAs channel device and 170mS/mm for a 3μm gate length InGaAs channel device with almost perfect pinch-off characteristics. However, more often the Si_3N_4/Si/GaAs and Si_3N_4/Si/Ge/GaAs structures MISFET devices show abnormal two peak transconductance behavior caused by the incomplete pinch-off. In order to find out the origin, high frequency C-V, G-V, and dc I-V characteristics investigations have been performed directly on these different structuress of devices. The research shows that Si_3N_4/Si/$In_{0.05}Ga_{0.95}As$/GaAs structure devices distinguish themselves by different generation-recombination mechanism dominating the loss. The absence of conductance peaks in depletion and weak inversion indicates that there are no significant interface states exisiting in the midgap of near midgap regions, and may explain why this kind of structure of devices does not have two peak phenomena observed.

Most recent effort was directed toward the improvement of the gate dielectric quality by reducing the bulk trap density, which is believed to be a primary factor in affecting the threshold voltage stability and the hysteresis. Silicon nitride films were chosen as a gate dielectric because of the larger dielectric constant afforded than that of silicon dioxide,

which results in a larger gate insulator capacitance and hence smaller threshold voltage shift - for the same defect trap charge- and larger transconductance as compared to SiO_2 itself. Stoichiometric silicon nitride (Si_3N_4) has been known to have the least bulk defects among the various forms of silicon nitride, and have both higher dielectric breakdown field and lower leakage current than non-stoichiometric films. In order to reduce the bulk trap density in the insulator, which would have the beneficial outcome of threshold voltage stabilization, we have optimized deposition conditions to yield stoichiometric silicon nitride established the process window within which stoichiometric silicon nitride films can readily be obtained. The optimized stoichiometric silicon nitride exhibited a refractive index of 1.9-2.0, Si/N solid ratio of 0.75, no excess Si-Si bond, and hydrogen concentration less than 3×10^{21} atoms/cm^3. A leakage current of less than 100pA/cm^2 at an electric field of 2MV/cm, a resistivity of larger than 4×10^{17} cm, and a breakdown strength of 6-11MV/cm at a current density of 1A/cm^2 characterized the properties of the films obtained. These properties of Si_3N_4 are comparable to the stoichiometric silicon nitride prepared by the thermal CVD method at high temperature (>700°C).

Silicon-nitrogen bond configuration is rather rigid and imperfections are not easily compensated for. In order to circumvent this problem we incorporated small amounts of oxygen in the films. The Si-O bonds can tailor themselves so as to avoid the formation of dangling bonds. Consequently, the breakdown strength and the leakage current of our dielectric films improved considerably. For example, the breakdown strength is consistently above 8 MV/cm. We found that the conduction mechanism in silicon nitride (SiN_x) and silicon oxynitride (SiO_xN_y) is a function of composition, namely the Si/N and/or N/O ratios in the film. We studied three different samples: Si-rich, stoichiometric, and oxynitride sample is dominated by the Fowler-Nordheim tunneling; the Si-rich sample by the Frenkel-Poole emission. On the other hand, the stoichiometric silicon nitride sample shows a Frenkel-Poole regime at intermediate fields and a Fowler-Nordheim regime at high fields. We are in the process of investigating the fundamentals behind these behaviors in terms of microstuctures in silicon nitride and oxide.

In a parallel effort, InP-based MIS structures were utilized to analyze the interface quality of the Si_3N_4/InP and Si_3N_4/Si/InP capacitors. Homoepitaxial layers of n-type InP were grown on n^+-InP substrates using In and PH_3 followed by the deposition of Si and Si_3N_4 in the ultrahigh vacuum connected UHVCVD system. The capacitor having pseudomorphic Si interlayer combined with low temperature deposition of the Si_3N_4/Si layer showed much improved interface quality with very small hysteresis(<10mV). An important observation in InP-based MIS interface is the pronounced frequency dispersion in the depletion-inversion region. This is under investigation, but suffice it to say that minority carrier generation is involved in some fashion.

In order to investigate GaAs surfaces further, we employed sulfide treatment which is applied by anodic means. Schottky contacts were formed on anodically treated n-GaAs. It was found that the Schottky barrier is lowered by at least 200meV due to the passivation of the surface of GaAs confirming a notable reduction in the interface trap density. The stability of the anodic sulfide passivation is studied in detail. The Schottky barrier height is not stable for samples treated at small current density (83A/cm^2) but much more stable for samples treated at large current densities (~1mA/cm^2). The stability of the passivation is sensitive to photon energy. For longer wavelength (λ=524nm) illumination, the passivation is rather stable, while for shorter wavelength (λ=325nm) illumination, the passivation is not stable. These can be explained by photon-assisted oxidation effect. In view of the C-V and PL measurements, the optimum anodic current density for passivation should be

1mA/cm^2. Comparing with the treatments by dipping samples into $(NH_4)_2S$ solution, the stability of anodic sulfide passivation technique with our high quality Si_3N_4 dielectric deposited by our ECR PECVD system, it is very possible to further improve our MIS structures.

We also carried out theoretical modeling of the current-voltage characteristics of MISFETs utilizing III-V materials such as GaAs, InGaAs, InP and their alloys. The modeling is general enough also to be applicable to the MISFETs from wide-bandgap nitridess (e.g., GaN and its alloys with InN and AlN). One of the objectives of this modeling is to provide guidelines to the experimental activities carried in parallel by experimentalists of our group. Our preliminary calculation based on analytical modeling demonstrates that the gate potential generated in both enhancement-type and depletion-type MISFETs. The calculation indicates that the inversion (accumulation) layer width in MISFETs ranges between 10 and 100Å depending on the doping and gate voltage, and that the interface surface states play an important role in determining the surface potential. A more accurate quasi two-dimensional model is being developed for determining the density of electrons and potential distribution for lowly doped and intrinsic semiconductor. It is expected to assist in exploring the possibility of ballistic current in very short channel MISFET. Initial efforts included a study of MIS diodes in order to calculate the effect of trap densities at the interface, which is especially important for GaAs based MISFETs.

In a summary, we have made significant progress in the development of new class of III-V MISFET devices.To date semiconductor dielectric with interface state densities in the mid 10^{10} cm^{-2} eV^{-1} already obtained. When the deposition conditions of the interface matching Si alyer and the dielectric are controlled carefully, hysteresis and most importantly the notorious frequency dispersion are reduced to the point that optimism for reliable devices can be had.

Selected List of publications supported by AFOSR

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